Sun 3 Architecture
A Sun Technical Report
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# 1 Hardware Architecture

Hardware architecture is the structure of a computer system visible to software. While the traditional goal of hardware architecture has been to allow software compatibility across multiple generations of systems, the design criteria of the Sun-3 architecture followed three additional goals: to build a family of workstations that is high performance, open, and cost-efficient.

## 1.1 Sun-3 Design Criteria

The Sun-3 architecture is high performance. Its family of workstations delivers from 1.5 to 4 million instructions per second (MIPS). The Sun-3 achieves this performance by utilizing the latest microprocessor, memory, cache technology, and by designing for maximum performance. In addition, high-end members of the Sun-3 workstation family provide optional accelerators that offer even greater performance for floating point operations and graphics processing. With its inherent high performance and optional accelerators, the Sun-3 family of workstations addresses application areas that previously required special-purpose computer architectures or large, expensive mainframe-level systems.

The Sun-3 architecture is open: It employs industry standards whenever possible. For those models that feature a system bus, the Sun-3 architecture uses the industry-leading 32-bit VMEbus, compatible with a large number of board-level components. For its disk interface, it uses the SCSI and SMD standards, compatible with a wide range of mass-storage devices. For data communication, Sun-3 workstations use Ethernet and RS-423 interfaces, and protocols that are compatible with international, industry, and de facto standards. The commitment to standards opens the Sun-3 for extensions and enhancements as they evolve in the marketplace. The use of standards also makes it easy to integrate Sun-3 workstations with customers' other systems requirements.

The Sun-3 architecture is cost-efficient. Since it is based on the latest VLSI technology, a complete Sun-3 workstation, including CPU, MMU, cache or main memory, video, networking, and standard input/output, fits on a single Eurocard. This integration at the component and system level not only lowers cost, but also increases reliability. In addition, the Sun-3 was specifically designed for high-performance "diskless" operation with networked servers, again lowering system cost and improving reliability.

At the time of this writing, the Sun-3 family comprises three series of workstations, each offering a number of configurations. (See Appendix A for more details.) This document primarily focuses

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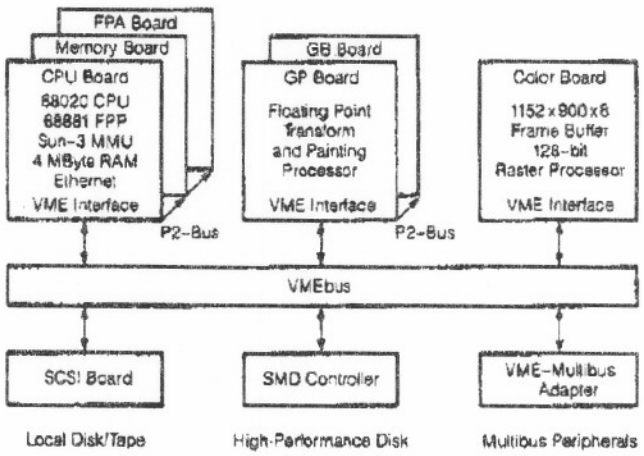


on the common features of the Sun-3 architecture, especially those points relating to its software compatibility. Only those features of the Sun-3 architecture already introduced are described in these pages. Although the Sun-3 architecture is well established, some features, such as increased CPU speeds, change. The latest specifications are always available by contacting Sun Microsystems.

## 1.2 System Architecture

The illustration below (Figure 1.1) graphically highlights the Sun-3 architecture using the Sun-3/160C color workstation as an example. The general-purpose computer is configured with a CPU board, Memory Expansion boards, Floating Point Accelerator (FPA), Graphics Processor (GP), Graphics Buffer (GB), color board, and mass storage.

*Fig. 1.1* *Sun-3/160C System Architecture*




The CPU (central processing unit) board contains the core elements of the workstation, which are the CPU, floating-point coprocessor, memory management unit, main memory, network interface, and standard I/O. The CPU board has a high-speed on-board bus which extends over the P-2 connector, providing a high-performance interconnection between these resources. Memory-expansion boards and the Floating Point Accelerator (FPA) board connect to the P2-Bus as well. The CPU board by itself is a complete monochrome workstation.

Other devices, such as the color frame buffer, the graphics processor, SCSI, SMD, and other I/O interfaces, address the CPU over the VMEbus. The color frame buffer connects to the VMEbus and can be directly accessed both from the CPU and from the Graphics Processor. Devices on the VMEbus, such as the Graphics Processor, may use their own private buses to other boards, such as the graphics buffer.

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The multiple-bus architecture of the Sun-3 allows data transfers in parallel on the internal buses and on the system bus, thereby greatly improving system performance.

*Fig. 1.2* *CPU Board Architecture*

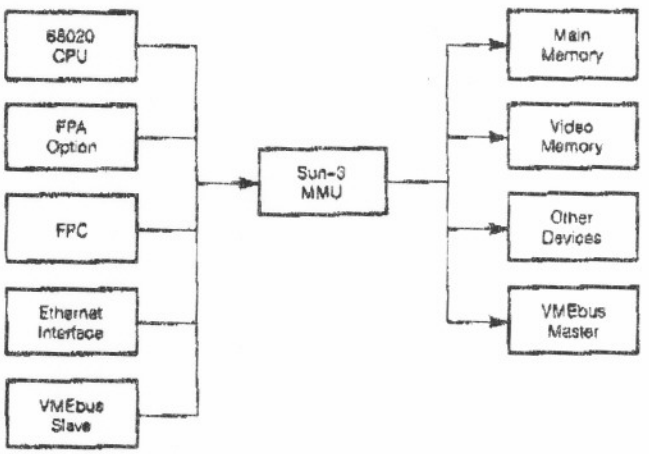



Figure 1.2 illustrates how the devices on the CPU board are interconnected in the Sun-3 architecture. The CPU sends a virtual address to the MMU, which translates it into a physical address located in main memory, video memory, I/O, or the VMEbus master interface.

The CPU, Ethernet, and VMEbus slave interfaces arbitrate for and share the virtual address bus. Since all addresses in the system pass through the MMU, all accesses are translated and protected in an identical fashion. Cache data receives identical protection.

The Sun-3 MMU provides the virtual to physical address translation, as well as protection, sharing, and memory allocation for multiple processes. The MMU uses a two-level segment/page translation and provides complete simultaneous mapping for eight processes with up to 256 megabytes of virtual address space for each process.

Besides those already mentioned, the CPU includes other standard devices. They include the EPROM, EEPROM, time-of-day clock, interrupt control, serial line I/O, keyboard/mouse I/O, and control registers that provide basic system functions.

## 1.3 CPU Architecture

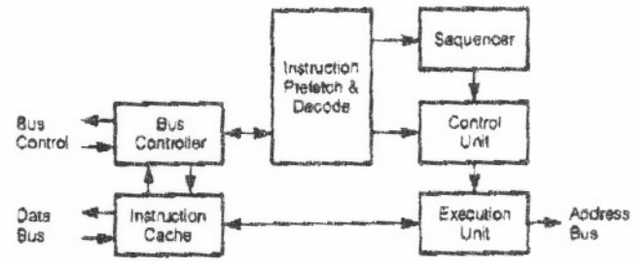
The CPU architecture includes the CPU itself, the floating point coprocessor, Sun's Floating Point Accelerator, the IDPROM, and several control registers.

### 1.3.1 The CPU

The Sun-3 uses the powerful Motorola 68020 single-chip microprocessor. The MC68020 includes a full 32-bit CPU, with 16 general-

purpose 32-bit data and address registers, two stack registers and program counters, a 256 byte on-chip instruction cache, and a high-speed 32-bit execution unit.

*Fig. 1.3* *MC68020 Block Diagram*




The bus controller loads instructions from the data bus into the decode unit and the on-chip cache. The sequencer and the control unit provide overall control. They manage the internal buses, registers, and execution unit.

The MC68020 uses an internal, three-stage pipeline for instruction processing. This pipeline allows concurrent processing for up to three consecutive instructions.

The CPU's on-chip instruction cache improves performance by storing active code segments. These instructions are executed directly from cache without requiring an external memory reference.

### 1.3.2 Floating Point Coprocessor

The Sun-3 architecture uses the Motorola 68881 floating point coprocessor. The MC68881 performs operations according to the IEEE 754 standard for binary floating point arithmetic. It features eight 80-bit floating point registers, three 32-bit control registers, and a coprocessor interface to the MC68020 that allows overlapped execution of 68020 and 68881 instructions.

### 1.3.3 Floating Point Accelerator

The Floating Point Accelerator (FPA) is a high-performance option for the Sun-3/100 and /200 series systems. The FPA increases floating-point performance over the floating point coprocessor by an average factor of four.

The FPA performs single and double precision floating point arithmetic according to the IEEE 754 standard. It implements the basic arithmetic functions of this standard as well as elementary transcendental functions.

The FPA is optimized for performance by being directly coupled to the CPU P2-Bus. CPU processing and FPA operations automatically overlap. A two stage pipeline and dual-ported registers further improve simultaneous operation of the CPU and FPA. Thirty-two sets of 32-bit floating point registers are built into the FPA.

The FPA is software transparent. That is, binary application programs are transportable between machines with and without the FPA option. To achieve the highest performance, however, applica-

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tions written for workstations without the FPA option should be recompiled when used with the FPA.

### 1.3.4 IDPROM and Control Registers

Every Sun-3 workstation contains a unique, sofrware readable IDPROM. The IDPROM is a 32-byte, nonmodifiable bipolar PROM. It stores individual information about the machine, such as the machine type, serial number, Ethernet address, and date of manufacturing.

The Sun-3 CPU includes control registers that assist the CPU with exception handling and with the overall control and initialization of the system. These registers are directly accessible to the CPU without going through the memory management unit.

## 1.4 Virtual Memory Architecture

The Sun-3 virtual memory architecture was designed specifically to support the demand paging requirements of large application programs. It provides mapping for processes up to 256 megabytes and features exceptionally fast context switching as well as a very large number of translation entries. It also supports virtual input/output procedures as well as direct virtual memory access from I/O devices.

Virtual memory, pioneered by the mainframes and superminicomputers of the 1970s, means that user programs can be larger than physical memory. This feat is accomplished by a storage hierarchy in which a virtual image of a program is stored in secondary storage while main memory only stores active program segments.

In paged virtual-memory schemes, memory is divided into equal size "pages." Each page of virtual memory is mapped separately into a page of physical memory. Active pages are brought in from secondary storage on demand ("demand paging"), replacing pages resident in memory that are not currently active.

### 1.4.1 Sun-3 MMU Features

The Sun-3 workstation family features the Sun-3 virtual Memory Management Unit (MMU). Sun's patented MMU has the following key advantages over other approaches to memory management:

1. *Large Working Set.* The Sun-3 MMU maps up to 32 megabytes of physical address translation entries simultaneously. For most applications, this approach provides complete mapping. The large working set increases performance substantially because translation entries do not have to be replaced during execution time. This is especially important for large programs used in artificial intelligence or computer-aided engineering applications. (Current Sun-3 systems support up to 16 Mbytes of physical address.)
2. *Rapid Context Switching.* Since the Sun-3 MMU stores eight separate translation contexts simultaneously, the CPU can

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switch between resident contexts with a single instruction without having to reload large tables. Rapid context switching is an important feature for enhancing interactive multiprocess applications, such as multiwindow activity, database updating, and networking.

3. *DVMA.* Direct Virtual Memory Access (DVMA™) means that I/O devices such as the network interface or the disk interface, as well as coprocessors, use virtual addresses to communicate with main memory. These references are translated, protected, and checked in identical fashion as those in the CPU. This process streamlines and insures the integrity of software on the system.

4. *Virtual Input/Output.* The Sun-3 applies the concept of virtual memory to input/output as well. I/O devices are represented as individually mapped virtual objects that can be directly mapped into a user's address space. User processes have fully protected direct access to I/O devices without operating system overhead.

5. *Pipelined Translation.* The Sun-3 MMU overlaps virtual-to-physical address translation with main memory access. This is done by using the (untranslated) page-address bits directly from the CPU for the row of main memory and the translated address bits form the column address. Thus, the Row Address Strobe (RAS) occurs in parallel, simultaneously with the translation of the virtual address of the Column Address Strobe (CAS). This feature is a Sun patent and results in the very fast memory cycle time of the Sun-3 architecture.

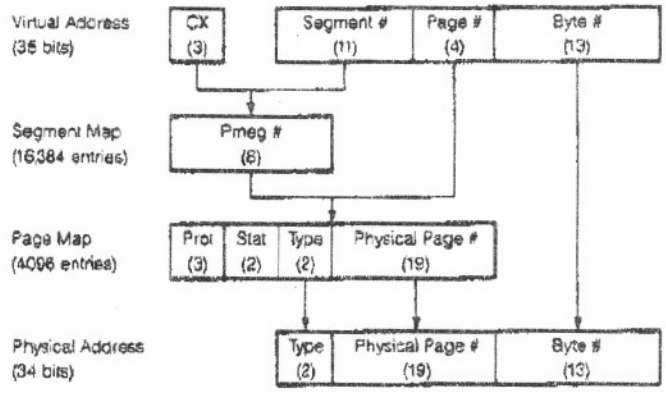
### 1.4.2 Sun-3 MMU Overview

The Sun-3 MMU consists of a context register, a segment map, and a page map. Virtual addresses from the processor are translated into intermediate addresses by the segment map, and then into physical addresses by the page map. The MMU uses a page size of 8 Kbytes and a segment size of 128 Kbytes. The MMU supports mapping of contexts with a virtual address space of 256 Mbytes each. Figure 1.4 illustrates the MMU layout.

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*Fig. 1.4* *Sun-3 Memory Mangement Unit*




1.4.2.1 Contexts

The Sun-3 MMU is divided into eight distinct address spaces or "contexts". The current context is selected by means of a 3-bit context register, which facilitates rapid task switching between multiple processes. The same context applies to both user and supervisor states.

1.4.2.2 Segment Map

The segment map has 16,384 entries. It is indexed by the three bits of the current context register and the 11 most significant bits of the virtual address, bits 17 through 27. Thus, the segment map is divided into eight contexts of 2048 entries each. Segment map entries are eight bits wide, pointing to a page map entry group, or pmeg.

1.4.2.3 Page Map

The page map contains 4096 page entries, each mapping an 8 Kbyte page. Page map entries are composed of a valid bit, protection field, type field, accessed and modified bits, and a page number. The page map is divided into 256 sections of 16 entries each. Each section is pointed to by a segment map entry.

*Protection Field:* The protection field has three bits: valid, write, and supervisor. The valid bit means that the page entry is valid and enables read and execute access to the page. The write bit allows write access to the page. The supervisor bit means that access is restricted to the supervisor state.

*Page Type Field:* The 2-bit, page-type field provides up to four physical address spaces, each starting at a physical address of 0. The four address spaces are main memory, I/O devices, 16-bit VMEbus, and 32-bit VMEbus.

*Statistic Field:* The statistic field has two bits: accessed and modified. As the name implies, these bits are set whenever a page is accessed or modified (written to). The statistics bits are automatically updated by the hardware.

*Physical Page Number Field:* The physical page number field generates the physical address of the page.

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## 1.5 Sun-3 Cache

The Sun-3 architecture optionally includes a high-performance cache. This cache is implemented on the high-end Sun-3 Series 200 and allows its MC68020 processor to execute with 0 wait states at 25 MHz for maximum performance.

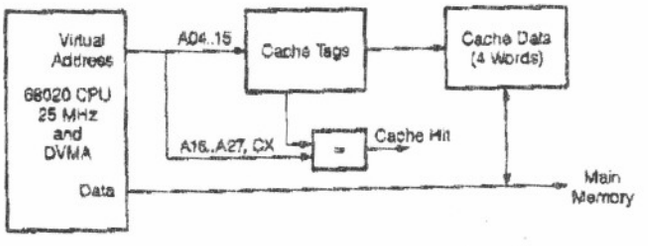
The Sun-3 cache is completely transparent to application programs. Existing applications will run and utilize the cache without modification.

The Sun-3 Cache is a virtual-address, direct-mapped, write-back cache. It is 64 Kbytes in size with 16 bytes lines (or 4 long words). The main benefits of this cache architecture are:

- Virtual-address, single-set organization makes the cache very fast and allows it to support a 25 MHz 68020 CPU with 0 wait states
- Large total size, block size, and write-back nature result in a very high hit rate to the cache. Measurements indicate that the average cache hit rate of the Sun-3 cache exceeds 97%.
- DVMA input/output cycles go through the cache the same way as CPU cycles, improving their performance as well.
- A combination of hardware and software flush mechanisms allows efficient operation of the cache when virtual addresses change
- Write-back support hardware permits modified cache blocks to be restored to main memory in parallel with cache accesses by the CPU (or DVMA)
- Aliasing, which is the mapping of different virtual addresses to the same physical address, is supported through a unique combination of hardware and system software.

Figure 1.5 shows a block diagram of the Sun-3 Cache as implemented on the Sun-3 Series 200. Whenever the CPU (or DVMA) accesses memory, the cache is checked first to determine whether the required word is in the cache. This is done with the low-order virtual address bits A4 through A15 as an index, selecting one of 4096 cache tag entries. Next, the high-order virtual address bits, A16 through A27, and the current context number are compared to the tag of the selected entry. If there is a match (hit) and the tag is valid, the CPU accesses the data in the cache with 0 wait states. If there is no match (miss) then the cycle proceeds to access data from main memory.

*Fig. 1.5 Sun-3 Cache*



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Using a parallel addressing path, the CPU starts the access to both the cache and to the memory management unit simultaneously. On a cache miss, the memory management unit has already translated the physical address for main memory and the memory access can start immediately.

## 1.6 Physical Device Architecture

The physical device architecture consists of main memory, standard devices, and the VMEbus. Physical devices are addressed by the CPU and other master devices are addressed through the memory management unit.

### 1.6.1 Main Memory

Sun-3 workstations have a minimum of 2 Mbytes of main memory. The maximum main memory is system dependent, ranging from 4 to 32 Mbytes, depending upon the workstation model.

Sun-3 workstations use high-speed 256 Kbit and/or 1 Mbit memory components and feature either memory error detection based on byte parity or single-bit error detection, depending upon the Sun-3 model.

On those Sun-3 workstations that offer memory expansion, the additional memory is accessed by the high-speed P2-Bus that interconnects the CPU board with the memory expansion boards.

### 1.6.2 Standard Devices

The Sun-3 architecture includes standard devices that provide basic functions for Sun-3 systems. These devices are provided directly on the CPU board and include:

- EPROM: stores system initialization code for booting and diagnostics
- EEPROM: stores configuration parameters of the system
- Time-of-Day Clock: provides a clock with battery backup
- Interrupt Register: controls the system interrupts
- Serial Line Interface: two highly programmable serial I/O channels with vectored interrupts for local terminals, modems, data communication lines, or other I/O devices
- Keyboard/Mouse Interface: provides a serial interface to these devices
- Ethernet Interface: transfers data directly into memory with DVMA. Certain Sun-3 models feature an integral Ethernet transceiver (Cheapernet) and others use an external transceiver.

### 1.6.3 Other I/O Devices

Other I/O devices that plug into the Sun-3 VMEbus include:

- SCSI Interface: for interfacing 5.25-inch disk and 1/4-inch tape peripherals

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- SMD Interface: for interfacing high-performance SMD disk drives
- 1/2-inch Tape Interface: for interfacing 1600 bpi and 6250 bpi tape drives
- Second Ethernet Interface: for configuring network gateways
- VME-Multibus® Adapter: for interfacing Multibus cards to Sun-3
- Asynchronous Line Multiplexer: for linking additional serial devices
- A dual-wide to triple-wide VME card adapter for use with VME boards in the Sun triple-wide card cage.
- IPC: An IBM PC-AT™ compatible coprocessor with optional floppy subsystem

## 1.7 VMEbus Interface

For implementations of the Sun-3 architecture that include a VMEbus, a full 32-bit VMEbus interface is provided. The VMEbus is dual-ported with a master and slave interface. The master interface provides access from the CPU to the VMEbus, whereas the slave interface provides access from the VMEbus to the main memory and expansion memory via DVMA..

The Sun-3 VMEbus interface has the following VME options.

- Address Bus Option: A32 MASTER, A32 SLAVE
- Data Bus Option: D32 MASTER, D32 SLAVE
- Timeout Period: 100 microseconds, excluding bus acquisition
- Arbiter Option: One (single level)
- Requestor Option: ROR (release one request)
- Interrupt Handler Options: IH (1-7)

The on-board arbiter can be disabled for use with other VME arbiters. Jumpers enable or disable individual interrupt levels. The VMEbus master interface can address the 16-bit, 24-bit, and 32-bit VME address space as well as the 16-bit and 32-bit data space. The VMEbus slave interface allows access from the VMEbus to the CPU on-board memory by responding to a range of VMEbus addresses and treating them as though they were a range of virtual addresses generated by the processor.

The VMEbus slave interface supports byte, word (16 bits), and longword (32 bits) transfers to physically existing main memory. Attempts to access nonexisting memory or otherwise protected memory signal a VMEbus error. This feature allows virtual coprocessors as VMEbus masters.

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Bus cycles from VMEbus masters normally interleave with bus cycles from the CPU to main memory. For very high-speed burst transfers, the VMEbus slave interface automatically enters a special "auto-lock-mode" in which the VMEbus master locks out the CPU. This increases the VMEbus bandwidth.

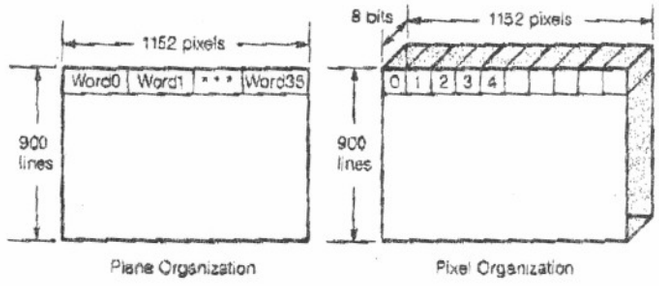
## 1.8 Graphics Architecture

The Sun-3 graphics architecture is based on raster graphics. Raster graphics means that every visible picture element ("pixel") on the screen has a corresponding storage location in memory. Raster graphics offers flexibility for the display of arbitrary objects, including variable width characters, foreign alphabets, mathematical symbols, lines, curves, shaded regions, and photographic images.

In a Sun-3 workstation, Display rasters are stored in dedicated regions of memory called *frame buffers* or video memory. Video memory appears as memory to the processor, but is dual-ported, with the second port serving the video refresh on the high-resolution monitor.

Sun-3 frame buffers are organized by plane and/or by pixel. The plane organization, used for monochrome applications, maps one bit of memory to one pixel. The pixel organization, used for color, maps one byte of memory to one pixel of the display.

*Fig. 1.6* *Sun-3 Display Organizations*




In the Sun-3 architecture, memory-mapped frame buffers are directly accessible from the main CPU. Some frame buffers feature additional raster operation ("Raster-Op") hardware to speed up raster operations. Raster-Op means that display rasters are modified or operated upon according to preselected functions. Depending on the frame buffer, the Sun-3 executes Raster-Op functions either in software, hardware, or firmware.

The Sun-3 video resolution is 1152 x 900 pixels that provides for square pixels on the display monitor[1]. For both monochrome and color workstations, the Sun-3 uses a high-resolution 19-inch display

[1] Some models feature an enhanced resolution of 1600 x 1280 pixles, or two million pixels on a screen.

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monitor that is refreshed, non-interlaced, 66 times per second. Ergonomic experiments have shown that this is the minimal refresh rate necessary to provide a flicker-free display and avoid operator fatigue.

### 1.8.1 Sun-3 Monochrome Frame Buffer

The Sun-3 monochrome frame buffer offers a screen resolution of 1152 x 900 pixels (standard) or 1600 x 1280 pixels (enhanced) with one bit per pixel. It is organized as 128 KByte (or 256 Kbyte) dual-ported memory with one port for the processor access and one port for display refresh. The monochrome frame buffer is implemented on the main CPU board.

### 1.8.2 Sun-3 Color/ Monochrome Frame Buffer

The Sun-3 color/monochrome frame buffer provides a screen resolution of 1152 by 900 pixels with an 8-bit per pixel color frame buffer, a separate 1-bit per pixel monochrome plane, and a 1-bit per pixel enable plane. Enable plane selction is pixel by pixel whether the color frame buffer or the monochrome frame buffer is displayed. This process allows color and monochrome windows to be displayed side by side on the same color screen.

An integral color map translates the 8 bits from the color frame buffer into 8 bits each for red, green, and blue, capable of over 16 million colors. The monochrome plane, if enabled, appears in black and white.

The Sun-3 color/monochrome frame buffer is implemented on the main CPU board and directly connects to the processor bus for maximum performance.

### 1.8.3 VME Color Frame Buffer

The VME color frame buffer provides a screen resolution of 1152 x 900 with 8 bits per pixel. An integral color map translates the 8 bits per pixel into 8 bits each for red, green, and blue, capable of generating over 16 million colors.

The VME color frame buffer has two addressing modes: plane and pixel. Plane mode accesses the frame buffer memory as eight separate bit-planes. This mode is compatible with the monochrome video architecture and is typically used for text and other raster operations. Pixel mode accesses the frame buffer as an array of 8-bit pixels. This mode is typically used for vector drawing, shading algorithms and other imaging related applications. Individual planes can be enabled and disabled in hardware.

The VME color frame buffer incorporates a set of custom Raster-Op processor chips. The eight Raster-Op chips, one processor per bit-plane, operate on up to 128 bits at a time. The maximum Raster-Op update rate is 46 million pixels per second. The Raster-Op processors perform any logical operation between a source, pattern, and destination register, and they return the result to the destination in the frame buffer. In addition, the Raster-Op processors perform bit shifting and masking functions, which allow users to shift the source words into alignment with the destination words before applying the logical Raster-Op. The Raster-Op processors operate

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The VME color frame buffer is located on a separate VME board that connects to the VMEbus. It is directly accessible both by the CPU and the optional Graphics Processor.

### 1.8.4 Graphics Processor and Graphics Buffer

The availability of fast bipolar processors and high-speed floating point chips has made it possible to build low-cost graphics pipelines from off-the-shelf components and achieve performance rivaling that of custom VLSI components. Sun's Graphics Processor (GP) board and a Graphics Buffer (GB) board improve the performance of graphics operations by a factor of 2 to 250 depending on the operation. The Graphics Processor accelerates the graphics performance of applications using Sun graphics libraries, such as Core, CGI, and GKS (see Chapter 8).

Using a two-stage pipeline and a floating point chip set, the Graphics Processor performs transformations, clipping, scaling, and rendering operations on vectors and polygons. The Graphics Processor supports graphics in windows, multiple processes access, area fill and copy operations. It clips to rectangle lists to overlapping windows, and features a shared memory ring buffer to handle multiple process windows. The Graphics Processor is a field-installable board-level subsystem for systems that have the VME color frame buffer. It consists of one or two VME boards, the Graphics Processor and the optional Graphics Buffer.

The Graphics Processor incorporates a dual processor architecture especially suited for high-performance graphics rendering. One processor, called the Viewing Processor, receives commands and parameters from the Sun-3 CPU and performs the floating point operations needed to transform the image from world coordinates into screen coordinates and also performs the clipping and scaling operations. The second processor, called the Painting Processor, renders the graphic data into the color frame buffer. The Painting Processor does this by manipulating the color frame buffer directly via the VMEbus, drawing vectors, filling polygons, and other tasks as commanded by the Viewing Processor. The Viewing Processor communicates to the Painting Processor via a first-in-first-out (FIFO) buffer.

The Graphics Buffer connects to the Graphics Processor via a local, high-speed bus. Each pixel in the color frame buffer has a 16-bit word of Z-depth value stored in the Graphics Buffer. The GP's Painting Processor, when rendering objects in 3-D, consults the GB location in the Z-plane memory corresponding to the pixels on the screen it is intending to write data to, then determines whether to write the new value in front of the object currently in the frame buffer, or to discard the pixel because it falls behind the pixel on the screen. A GP is a prerequisite to install a Graphics Buffer.

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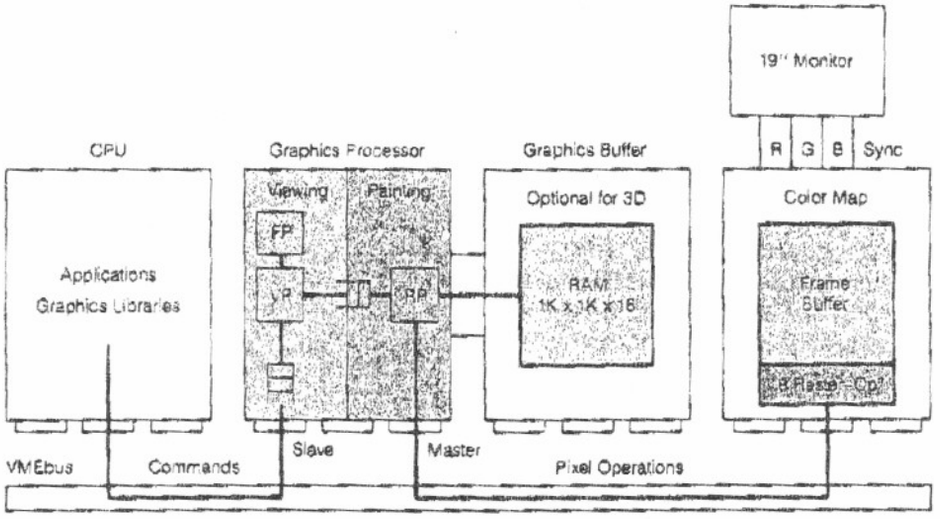



*Fig. 1.7* *Sun-3/160C Graphics Subsystem*

1.8.4.1 Performance

The following table summarizes the performance of a Sun-3/160C with a GP/GB. All operations include transformations, clipping, scaling, and, for polygons, Gouraud color shading and hidden-surface elimination.

| Operation | Performance |
|---|---|
| 2-D Short vectors (transformed, clipped, scaled) | 40,000 per second |
| 3-D Short vectors (transformed, clipped, scaled, shaded) | 25,000 per second |
| Vector drawing rate | 500 nanoseconds per pixel |
| Vector drawing rate | 2.0 Mpixels per second |
| 3-D Point transforms | 8.9 microseconds per point |
| 3-D Shaded polygons | 1600 per second |
| Area fill rate | 33 Mpixels per second |

1.9 Diagnostics

To facilitate diagnostics, all devices in the system provide readback of their content, allowing complete software checkout of the machine. Many system devices also provide self-test modes or other diagnostic features.

On every power-on, code in the boot EPROM checks the functionality of the CPU board before allowing the UNIX® operating system to take control. Error messages are signaled on the video display, the serial line, or the diagnostic display when a

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malfunction occurs. Elective diagnostics for the video display, the Ethernet, memory, serial ports, keyboard, and all other boot paths are available.

Three additional Sun-3 features are dedicated to diagnostics: the diagnostic display, the diagnostic switch, and the watchdog circuit. The diagnostic display is eight LEDs on the back of the machine for the display of error messages while the machine is booting. The diagnostic switch allows a user to put the system in a special diagnostic mode, bypassing the normal system booting sequence. The watchdog circuit resets the system should the CPU ever halt, allowing automatic restart in case of catastrophic failure.

## 1.10 Mass Storage Architecture

The Sun-3 architecture comprises both high-performance diskless and local mass-storage configurations. With Ethernet being a standard on all Sun-3 computers, networks of Sun workstations and servers can be distributed across a network with mass storage options according to cost/performance requirements.

### 1.10.1 Diskless Workstations

A diskless workstation accesses its mass storage via the Ethernet from a Sun fileserver. The Ethernet, with a 10 megabit per second data transmission rate, provides sufficient bandwidth to serve as a link between diskless workstations and servers. To facilitate diskless operation, the Ethernet interface in the Sun-3 architecture was designed for maximum throughput which was achieved by two design choices. First, the Ethernet interface transfers the data directly between the network and main memory. Second, the interface is able to accept any number of back-to-back packets from the network without losing any of them. With these capabilities, the networking hardware in the Sun-3 architecture performs diskless input/output at speeds comparable to local mass storage configurations.

### 1.10.2 Disk Drives

The Sun-3 family offers a range of disk drive options and attendant performance characteristics. Currently available options include the following:

| Size | Capacity | Seek-time | Interface | Transfer Rate |
|---|---|---|---|---|
| 5.25 inches | 85 MB | 35 msec | SCSI | 0.6 MByte/sec |
| 8 inches | 337 MB | 20 msec | SMD | 2.4 MByte/sec |
| 10.5 inches | 689 MB | 18 msec | SMD | 2.4 MByte/sec |

The SCSI (Small Computer Systems Interface) provides an industry-standard, high-level interface that works with disks as well as tapes and other devices. The SMD (Storage Module Drive) interface is the industry standard for high performance, large capacity disk drives. The capacity figures noted in the table above reflect unformatted space on drives.

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1.10.3 Tape Drives

For backup purposes, the Sun-3 workstations have three options.

| Size | Density | Capacity | Interface |
|---|---|---|---|
| 1/4-inch | 10,000 bpi | 60 MBytes | SCSI |
| 1/2-inch | 1600 bpi | 30 MBytes | Pertec |
| 1/2-inch | 6250 bpi | 130 MBytes | Pertec |

1.11 Conclusion

Based on the latest microprocessor technology, the Sun-3 architecture achieves a significant increase in performance over previous workstation architectures. Optional floating point and graphics accelerators provide even more speed for those applications.

With its performance, large virtual memory space, and ability to handle large amounts of physical memory, Sun-3 systems can run applications that previously required mainframe or special-purpose computer architectures.

The use of industry standards makes the Sun-3 architecture expandable and compatible with current technology. It provides a migration path to future technologies. It also provides the flexibility to easily adapt the Sun-3 to specific customers' requirements.